AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of claims:

1. (Cancelled)

2. (Currently Amended) ~~The clock generating device of claim 1,~~ A clock generating device for generating a clock signal synchronizing with a wobble signal, which includes address information for a predetermined period, the clock generating device comprising:

a PLL circuit for generating an oscillation signal in accordance with the difference between the phase of a wobble signal and the phase of a clock signal and for generating the clock signal by synchronizing the oscillation signal with the wobble signal; and

a detection circuit, connected to the PLL circuit, for monitoring the wobble signal, detecting the predetermined period of the wobble signal that includes the address information, and holding the frequency of the oscillation signal of the PLL circuit in accordance with the detection, wherein the detection circuit includes:

a hold signal generator for generating a first hold signal that holds the frequency of the oscillation signal of the PLL circuit during a first period in accordance with the detection, and a second hold signal that holds the frequency of the oscillation signal of the PLL circuit during a second period in accordance with the detection, which differs from the first period; and

a signal selector, connected to the hold signal generator, for providing the PLL circuit with either one of the first and second hold signals.

3. (Original) The clock generating device of claim 2, wherein the first period is shorter than the predetermined period, and the second period is longer than the predetermined period.

4. (Previously Presented) The clock generating device of claim 2, wherein the cycle of the wobble signal changes with at least two timings in accordance with the address information of the predetermined period, and the hold signal generator generates a first hold signal for holding the frequency of the oscillation signal of the PLL circuit during a period between a first timing and a second timing, at which the cycle of the wobble signal changes.

5. (Previously Presented) The clock generating device of claim 2, wherein the cycle of the wobble signal changes during the predetermined period, and the hold signal generator generates the second hold signal for holding the frequency of the oscillation signal of the PLL circuit during the second period, which is longer than the first period of the first hold signal, from a timing at which the cycle of the wobble signal changes.

6. (Original) The clock generating device of claim 2, further comprising:

a synchronization protection circuit, connected to the detection circuit, for performing counting in accordance with the wobble signal, estimating the predetermined period during which the address information is included in the wobble signal, and generating a synchronization protection signal in accordance with the estimated period, the signal selector of the detection circuit providing the PLL circuit with one of the first hold signal, the second hold signal, and the synchronization protection signal.

7. (Original) The clock generating device of claim 6, wherein the PLL circuit includes:

a phase comparator circuit for generating a phase difference signal in accordance with the difference between the phase of the wobble signal and the phase of the oscillation signal; and

a charge pump, connected to the phase comparator, for generating an output signal in accordance with the phase difference signal, wherein at least one of the phase comparator and the charge pump stops functioning in response to one of the first hold signal, the second hold signal, and the synchronization protection signal.

8. (Original) The clock generating device of claim 7, further comprising:

a frequency divider, connected to the phase comparator, for generating a divisional signal by dividing the oscillation signal by a predetermined dividing ratio, and providing the divisional signal to the phase comparator, the dividing ratio being changed in accordance with the cycle of the wobble signal.

9. (Original) The clock generating device of claim 2, wherein the PLL circuit includes:

a phase comparator circuit for generating a phase difference signal in accordance with the difference between the phase of the wobble signal and the phase of the oscillation signal; and

a charge pump, connected to the phase comparator, for generating an output signal in accordance with the phase difference signal, wherein at least one of the phase comparator and the charge pump stops functioning in response to one of the first and second hold signals.

10. (Original) The clock generating device of claim 9, further comprising:

a frequency divider connected to the phase comparator, for generating a divisional signal by dividing the oscillation signal by a predetermined dividing ratio, and providing the divisional signal to the phase comparator, wherein the dividing ratio is changed in accordance with the cycle of the wobble signal.

11. (Cancelled)

12. (Currently Amended) ~~The clock generating device of claim 11, further comprising:~~

A clock generating device for generating a clock signal synchronizing with a wobble signal that includes address information during a predetermined period, wherein the cycle of the wobble signal changes with at least two timings in accordance with the address information of the predetermined period, the clock generating device comprising:

a PLL circuit for generating an oscillation signal in accordance with the difference between the phase of the wobble signal and the phase of the clock signal and for generating the clock signal by synchronizing the oscillation signal with the wobble signal;

a monitor, connected to the PLL circuit, for monitoring the wobble signal, wherein the monitor generates a first hold signal that holds the frequency of the oscillation signal of the PLL circuit during a first period between a first timing and a second timing, at which the cycle of the wobble signal changes, and a second hold signal that holds the frequency of the oscillation signal of the PLL circuit during a second period, which is longer than the first period of the first hold signal measured from the first timing;

a signal selector, connected to the monitor, for providing one of the first and second hold signals to the PLL circuit; and

a synchronization protection circuit~~, connected to the detection circuit,~~ for performing counting in accordance with the wobble signal, estimating the predetermined period during which the address information is included in the wobble signal, and generating a synchronization protection signal in accordance with the estimated period, the signal selector of the detection circuit providing the PLL circuit with one of the first hold signal, the second hold signal, and the synchronization protection signal.

13. (Original) The clock generating device of claim 12, wherein the PLL circuit includes:

a phase comparator circuit for generating a phase difference signal in accordance with the difference between the phase of the wobble signal and the phase of the oscillation signal; and

a charge pump, connected to the phase comparator, for generating an output signal in accordance with the phase difference signal, wherein at least one of the phase comparator and the charge pump stops functioning in response to one of the first hold signal, the second hold signal, and the synchronization protection signal.